REMARKS

Applicants respectfully request reconsideration and withdrawal of the rejections of the claims.

1, 3-6, 8-13, 15-18, 20-23, 25-27 and 41-56 currently are pending. By the present response, claim 49 is amended to recite that a rare gas element having a concentration gradient is contained in the semiconductor layer.

In the Office Action, the Examiner maintained the rejection of claims 1, 3-6, 8-13, 15-18, 20-23, 25-27, 41-56 under 35 U.S.C. 112, first paragraph, as allegedly failing to comply with the written description requirement. Specifically, in response to Applicants' arguments directed to the Examiner's allegation that there is no enabling description of a channel region with an amorphous layer and a crystalline layer, the Examiner contends:

> Figures 2A-2G clearly show that the amorphous layer 206 is removed and does not comprise the channel layer 204, 208, 213 which layer clearly does not comprise an amorphous layer. Recitations in the original disclosure stating that the channel layer comprises an amorphous layer and a crystalline layer are contradictory to the process description shown in figures 2A-2G and are not considered enabling or a proper written description for a channel with an amorphous and crystalline layers. (See, page 2, lines 10-16.)

On page 3 of the Action, the Examiner requests Applicants to point out where in Figures 2A-2G there is any enablement, or any reason to conclude that there is any enablement for an amorphous channel layer. Applicant responds as follows:

As pointed out in the response dated March 28, 2005, lines 19-22 of page 5 of the specification do support such a feature, as follows:

> The upper layer in the channel region is a semiconductor film having an amorphous or crystalline structure. On the other hand, the lower layer in the channel region is a semiconductor film having a crystalline structure.

Moreover, Applicants pointed out that original dependent claim 13 (now cancelled), which recited "wherein the second semiconductor layer has an amorphous layer," provides further support for such a feature.

Furthermore, Applicants do not disagree with the Examiner's contention that the amorphous layer 206 formed over the crystallized semiconductor film 204, as shown in Figure 2C, is removed and does not comprise the channel layer 213 shown in Figure 2G. In the example of the invention shown in Figures 2A-2G, an amorphous layer is created in the upper region of the semiconductor film 204, and thus also in the later formed channel layer

213 (e.g., see page 11, lines 16-17), by way adding a rare gas element by an ion doping technique or ion implantation technique. For example, starting at line 15 of page 8, Applicants' specification describes implanting rare gas ions into the amorphous layer 206. This region is shown as a crosshatched area in the upper portion of layer 204 of Figures 2D, 2E and 3 (e.g., see lines 6-10 of page 9), in semiconductor layer 208 of Figure 2F, and in channel region 213 of Figure 2G.

It appears that the Examiner does not appreciate that adding a rare gas element to an upper region of a semiconductor layer as described in Applicants' specification would result in that region becoming amorphous. For example, in the Office Action dated December 27, 2004, the Examiner alleges, "There is no recitation that the upper portion of 202 implanted with rare earth ions is 'amorphous' or anything but the same crystallinity as the lower portion." It is respectfully submitted however, that one of ordinary skill in the art would have understood, after reading Applicants' original disclosure, and using his or her knowledge of the applicable arts, that a semiconductor film implanted with rare gas element, as described in specification, would have resulted in creating an amorphous layer in an upper area of a semiconductor film. In this regard, Applicants respectfully direct the Examiner's attention to U.S Patent No. 5,962,871 to Zhang et al., U.S. Patent No. 5,318,661 to Kumomi, and U.S. Patent No. 5,399,883 to Baliga, which demonstrate this type of effect.[1]

For example, the Zhang et al. patent teaches that implanting silicon ions into the whole surface of a silicon film makes it amorphous (e.g., see column 7, line 56 to column 8, line 16). The Kumomi patent teaches that the crystal nuclei is made amorphous by implanting silicon ions (e.g., see column 5, line 66 to column 6, line 4). Although silicon ions are used both in Zhang et al. and Kumomi, Applicants contend that the added rare gas element of the present invention has the same effect. Moreover, the Baliga patent teaches performing argon ion implantation to form an amorphous region in a semiconductor (e.g., see column 7, lines 26-40). In view of these teachings, it is respectfully submitted that one of ordinary skill in the art would have understood, that a rare gas element added to a

[1] These references are listed in a PTO Form 1449 attached hereto. The Examiner is requested to indicate consideration of these documents by returning an initialed copy of the PTO Form 1449 in the next communication to Applicants.

semiconductor film as described in Applicants' description would create an amorphous layer in an upper region of an otherwise crystallized semiconductor film.

With respect to claims 45-56, the December 27, 2004 Office Action also asserts that there is no original disclosure teaching how to make a bottom gate device nor any language in the original disclosure reciting the claim language. However, Applicants' disclosure contemplates applications of the present invention that involve, among other things, a bottom gate type device or forward stagger type device (see, page 12, lines 16-19). Furthermore, as Applicants' March 28th response points out, it has been held that precise recitation of the claim limitation in disclosure is not a requirement for "written description" to be satisfied, i.e., the invention does not have to be described *ipsis verbis* in order to satisfy the description requirement of §112. It is respectfully submitted that those skilled in the art would have realized that the inventors had in their possession, from knowledge in the art of processes used in making such devices and Applicants' original disclosure, the invention as defined in claims 45-56. More specifically, those skilled in the art would have realized the claimed invention in such device applications in which a semiconductor layer is formed over an electrode and containing a rare gas concentration gradient as set forth in claims 45-56 (also, see Figures 2A-2G, Figure 3 and the corresponding description at pages 5-12 of the application).

As instructed in MPEP §2163.04, the Examiner must provide a reasonable basis to challenge the adequacy of the written description. This initial burden on the Examiner involves presenting a preponderance of the evidence why a person of ordinary skill in the art would not recognize in Applicants' disclosure a written description of the invention set forth in claims. It is respectfully submitted that the allegations of inadequate written description provided by the Examiner are not founded in fact or reasoning to explain why persons skilled in the art would not recognize in the disclosure a description of the invention defined by the claims. Absent such a provision or showing, the rejection should be withdrawn.

The rejection also asserts that the pending claims are not enabled by Applicants' disclosure. However, the Office does not present reasons why a skilled artisan would have been subject to undue experimentation to practice the invention, which is required in establishing whether the specification adequately describes how to make and how to use the invention being claimed under 35 U.S.C. §112, first paragraph. This test for enablement was

set forth in the Supreme Court decision *Mineral Separation v. Hyde*, 242 U.S. 261, 270 (1916) as: "Is the experimentation needed to practice the invention undue or unreasonable?" *In re Wands*, 858 F.2d 731, 737, 8 U.S.P.Q.2d 1400, 1404 (Fed. Cir. 1988) confirms this is still the standard. See also MPEP 2164.01. In this instance, it is not clear that any undue experimentation would be required as more fully explained below. As identified in MPEP 2164.01(a) the undue experimentation factors include, but are not limited to:

(a) the breadth of the claims;

(b) the nature of the invention;

(c) the state of the prior art;

(d) the level of one of ordinary skill;

(e) the level of predictability in the art;

(f) the amount of direction provided by the inventor;

(g) the existence of working examples; and

(h) the quality of experimentation used to make and use the invention based on the content of the disclosure.

It is respectfully submitted that none of these factors have been adequately addressed by the Examiner in connection with undue experimentation. Insofar as the initial burden rests on the Examiner to provide reasons for lack of enablement, and the Examiner has provided no explanation regarding any of these factors, it is respectfully submitted that this rejection must fail, as the record does not establish a *prima facie* case of unpatentability. *In re Wright*, 999 F.2d 1557, 1562, 27 USPQ2d 1510, 1513 (Fed. Cir. 1993).

As noted in MPEP 2164.01(a), a conclusion of lack of enablement means that, based on the evidence regarding each of the above factors, the specification, at the time the application was filed, would not have taught one skilled in the art how to make and/or use the full scope of the claimed invention without undue experimentation. It is not evident that any experimentation need be done to carry out the present invention, let alone undue experimentation. To the contrary, because the semiconductor art is well a developed and predictable art, it is respectfully submitted that those having skill in this art would understand how to apply the exemplary techniques described in Applicants' original disclosure to various disclosed applications without undue experimentation. For instance, it is submitted that one of ordinary skill in the art would have understood how to make and use the invention as set

forth in claims 45-56, which are directed to devices in which a semiconductor film is formed over an electrode (e.g., a transistor including a bottom gate). The application of Applicants' disclosed techniques to such known device architecture types would have been readily apparent to those skilled in the art without undue experimentation. Additionally, it is respectfully submitted that those skilled in the art would recognize, from Applicants' disclosure, how to make a device having a semiconductor layer including a portion or layer containing a rare gas element, and that this portion or layer would have less degree of crystallinity than portion or layer of the film that does not include the added rare gas, as set forth in claims 1, 6, 11, 18 and 23.

For at least these reasons, the rejection under Section 112 is believed improper and should be withdrawn.

The final Office Action also maintained the rejection of claims 1, 3-6, 8-13, 15-18, 20-23, 25-27, 41-56 under 35 U.S.C. 102(b), as allegedly being anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over the Henley patent. In connection with this rejection, the Examiner asserts, at page 3, that Applicants' arguments were not considered persuasive, for the following reasons:

In response to Applicants' arguments that Henley fails to show a channel having a first and second portion with different crystallinities, as recited in independent claims 1, 6 and 18, the Examiner asserts that the term "channel region" is a mere label and can be defined in Henley as comprising all the layers 806 as shown in Figure 8. Applicants respectfully submit that the Examiner's overly broad interpretation of the claim term "channel region" is not reasonable in view of the meaning this term has attained in the art, especially when read in light of the specification. While it is noted that the PTO is given latitude to interpret claim terms broadly, MPEP §2111 instructs that the "PTO applies to verbiage of claims the broadest *reasonable* meaning of the words in their ordinary usage as they would be understood by one of ordinary skill in the art, taking into account whatever enlightenment by way of definitions or otherwise that may be afforded by the written description contained in applicant's specification" (citing *In re Morris*, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997)). In this regard, those skilled in the semiconductor art would recognize that a "channel region" means a semiconductor path in which current flows. It is respectfully submitted that Applicants use of this term in the specification and claims is

consistent with its ordinary usage in the art. Applicants also submit that one of ordinary skill in the art would not have considered the gettering layer 807 of Henley and the layer below the gettering layer 807 to comprise a "channel region" within any reasonable interpretation of this term. At best, Henley discloses an active layer 805, which is a region where active devices are formed. However, Henley does not describe or suggest that the active layer includes a first portion and a second portion with different crystallinities as claimed. The rejection, therefore, fails to establish a *prima facie* case of either anticipation or obviousness. Thus, Applicants submit that independent claims 1, 6 and 18 are allowable.

With respect to independent claim 11, the Henley patent does not disclose the claimed combination of features including a first semiconductor layer, a second semiconductor layer on the first semiconductor layer, an insulating film in contact with the second semiconductor layer, where the second semiconductor layer includes the rare earth element having a concentration gradient, and the crystallinity of the first semiconductor layer is higher than that of the second semiconductor layer. For instance, the Figure 8 embodiment of the Henley patent relied upon in the Action for allegedly disclosing all claimed features shows layer 807 including a rare gas. However, this layer is not in contact with an insulating film, which is in contact with an electrode. Hence, the Henley patent fails to describe or suggest each and every feature recited in Applicants' claim 11.

Applicants also contend that the Henley patent fails to disclose the combination of features set forth in independent claim 23.

In connection with independent claims 45, 49 and 53, the Examiner asserts that there is no particularly claimed concentration gradient that would in any way structurally distinguish over the concentration gradient of Henley. However, even if one were to consider, for the sake of argument, that the gettering 807 contains a "concentration gradient of noble gas" as stated in the Office Action, the Henley patent still would not teach or suggest the combination of each and every feature set forth in independent claims 45, 49 and 53. For example, claim 45 recites that a device includes an electrode over an insulating surface, an insulating film over the electrode, a semiconductor layer having at least a source region, a drain region and a channel region over the electrode with the insulating film interposed therebetween, and that the channel region contains a rare gas element having a concentration gradient. In contrast, the Henley patent is directed to providing a gettering layer an SOI

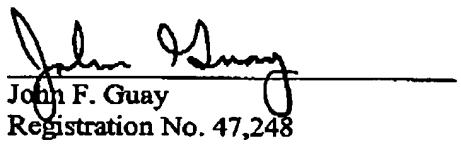
wafer (e.g., see column 1, lines 14-16 and column 2, lines 20-24). More specifically, it describes gettering layers in a SIMOX wafer, a wafer-bonded SOI wafer, and a wafer-bonded SOI wafer. It is respectfully submitted, however, that there is no teaching or suggestion in Henley that would have led one of ordinary skill in the art to modify the described *wafers* to include a channel region over an electrode with the insulating film interposed therebetween as set forth with the other features recited in claim 45. The Examiner's assertion on page 4 of the December 23, 2005 Office Action that "[t]he 'bottom' gate independent claims are considered obvious alternatives to the top gate structures as applicant has stated that they are obvious variations of a top gate device" does not remedy the shortcomings of Henley because there is no suggestion in Henley and the Examiner's allegation regarding "obvious variations" for forming these types of devices in the particular wafers discussed in Henley. Contrary to any such allegation, Henley only shows electrodes formed on the surface of an SOI wafer.

For at least these reasons, it is respectfully submitted that there is no motivation present in the Henley patent and the allegations of stated "obvious variations" that would have let one of ordinary skill in the art to make the modifications of the Henley device that would have been necessary to arrive the claimed invention. As instructed in MPEP §2143, such motivation for combining is a required criterion for establishing a *prima* facie case of obviousness. Because the Office has not met this requirement, claim 45 is considered allowable. A similar rational applies to each of claims 49 and 53, and thus these claims also are considered allowable.

The remaining claims depend from one of claims 1, 6, 11, 18, 23, 45, 49 and 53, and are therefore allowable at least for the above reasons, and further for the additional recited features.

From the foregoing, Applicants respectfully request reconsideration and withdrawal of all the pending rejections.

Respectfully submitted,



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